Rishav Raj

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EDUCATION

BIRLA INSTITUTE OF TECHNOLOGY, MESRA
BTECH in Electrical & Electronics
2018-2022 | Mesra, Ranchi
• CGPA: 8.46

DELHI MODEL PUBLIC SCHOOL
CBSE XIIth Board | 2016-2018
• Percentage: 91.4%

PATNA CENTRAL SCHOOL
CBSE Xth Board | 2005-2016
• CGPA: 10

SKILLS

HDL/HVL
• System Verilog
• Verilog
TB Methodology
• UVM
Scripting Language
• Basics of Perl, TCL, Python
Tools
• Synopsys VCS
• DVE, Verdi
• coreTools(IP Packaging)
Protocols
• AMBA APB, AHB.
• SSI, SPI
Other Skills
• HTML, CSS, JavaScript
• Front-End Web Development

LINKS

Website:// **rishavraj.tech**
LinkedIn:// **rishav-raj**
Github:// **Rishav Raj**

HOBBIES

• Robotics
• Trading
• Chess
• Cricket

EXPERIENCE

SYNOPSYS | Senior Engineer, ASIC Digital Design Verification
January 2022 - Present | Bengaluru, India

Higher SPI Slave Frequency Support :: SSI Controller.
• Verified the functionality of Baud Rate = 1 to enable synchronous operation of SSI controller and SPI slave device at maximum clock frequency.
• Developed timing-sensitive testcases to ensure stability, correct data shifting, and protocol compliance at high frequency. Also verified all the existing SSI controller features with new baudrate support.
• Driven functional coverage to a closure with 100 cross coverage with existing features.

Dynamic Wait State Support :: SSI Controller.
• Led verification for the Dynamic Wait State feature to allow latency tolerance in SSI communication with slower slaves.
• Built UVM testbench from scratch and implemented sequences simulating dynamic wait behaviors under varying latency conditions.
• Delivered coverage closure and first-pass success for customer tape-out.

Data Mask Enhancement :: SSI Controller
• Verified the Data Mask feature in Synopsys DWC SSI IP to ensure accurate selective write masking for enhanced memory protection and protocol compliance.
• Modified UVM testbench to support flexible data masking and integrated new checkers for masked data validation.

Clock Stretching Support in SSI Duplex Mode :: SSI Controller
• Verified clock stretching functionality during full-duplex TX_RX transfers to enable slave-side flow control.
• Updated UVM sequences and added scoreboard logic to verify correct pause/resume behavior and data alignment.
• Achieved complete coverage for various timing and backpressure scenarios.

Other Verification Projects
• **APB Register programming Support** - Verified integration of APB interface for register programming alongside existing AHB support.
• **SPI Sideband Signal Support** - Verified addition of xSPI sideband signals (RESET#, HRESET#, INT#) to support advanced peripheral signaling.
• **XIP Address Decoding Support** - Verified the XIP address decoding logic to support execute-in-place functionality from external flash via SSI.

ACADEMIC PROJECTS AND POR

• **Ball Balancing Bot (E-Yantra)** 2-DOF autonomous ball-balancing platform} which balances the ball in the center of the platform and upon a disturbance, the ball is returned back to the center.
• **Spyder Bot** - A Bluetooth controlled quadruped bot capable of walking in all terrain,even discontinuous paths with ease,actuated with help of 8 servo motors and controlled using arduino UNO.
• **Vice President** and **Vice Captain** at Robotics Club Robolution.
• **Web-D Lead** at Google Developer Student Club